Introduction to DFT

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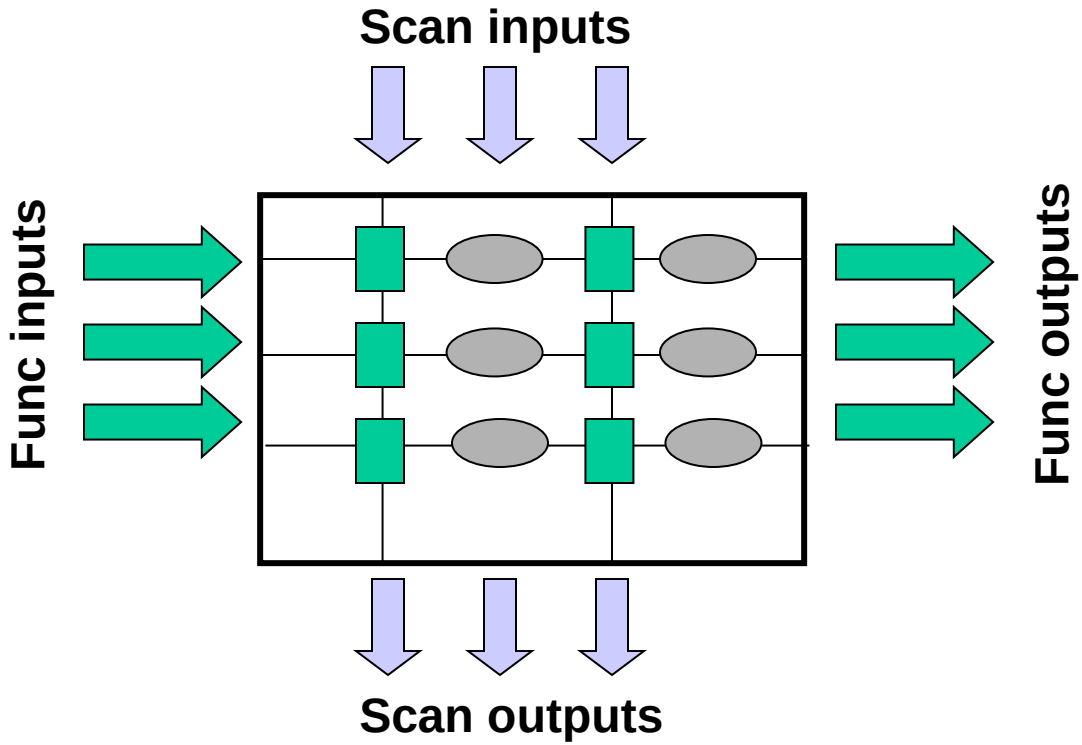
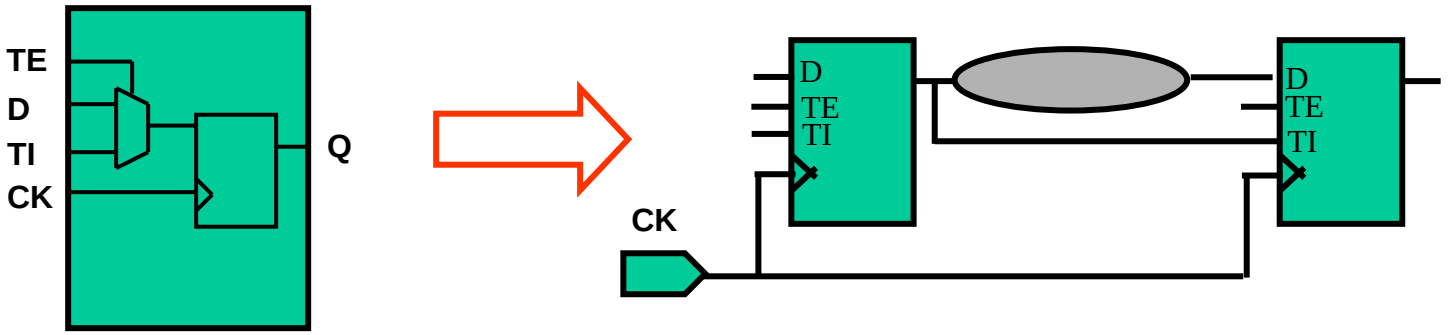
Internal Scan Concept

- Used to get access to all internal chip registers:



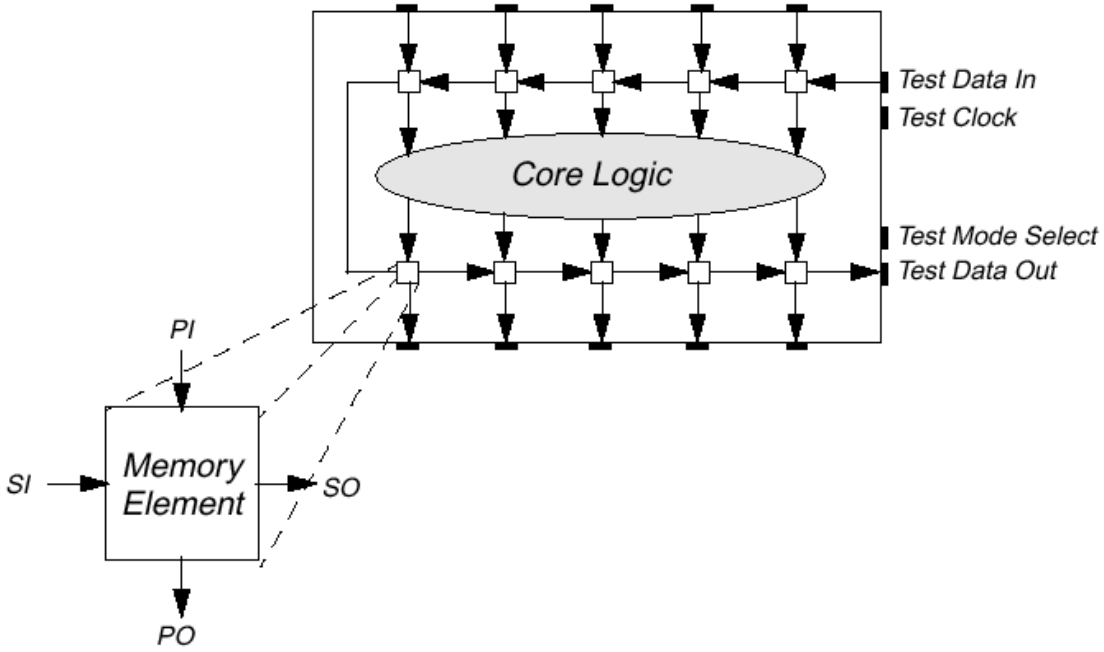
MuxScan Design

- MuxScan: use one clock for Func and Test mode
- TE signal selects mode
- In test mode reg-to-reg combinatorial logic is bypassed

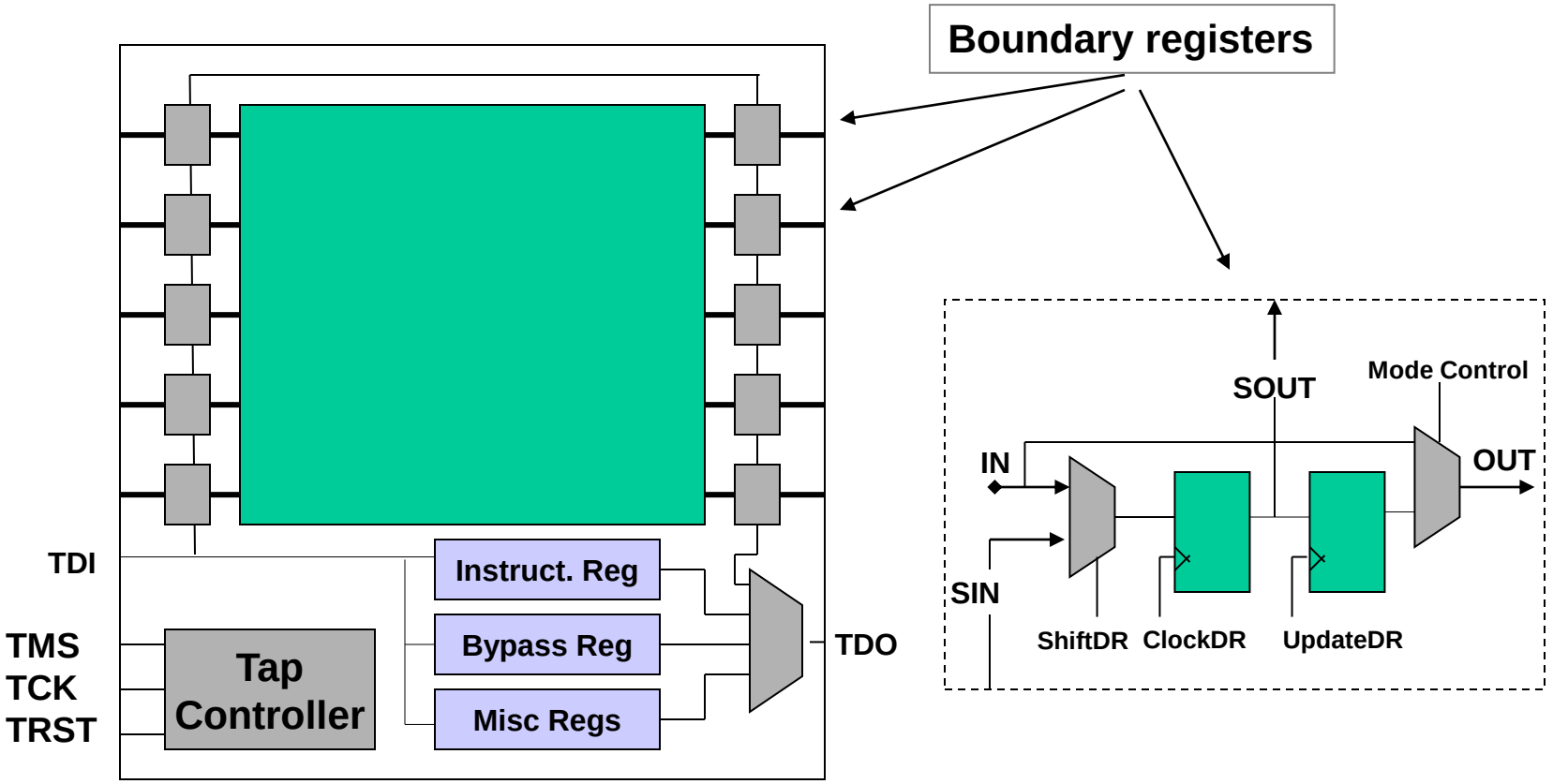


Boundary Scan Principles

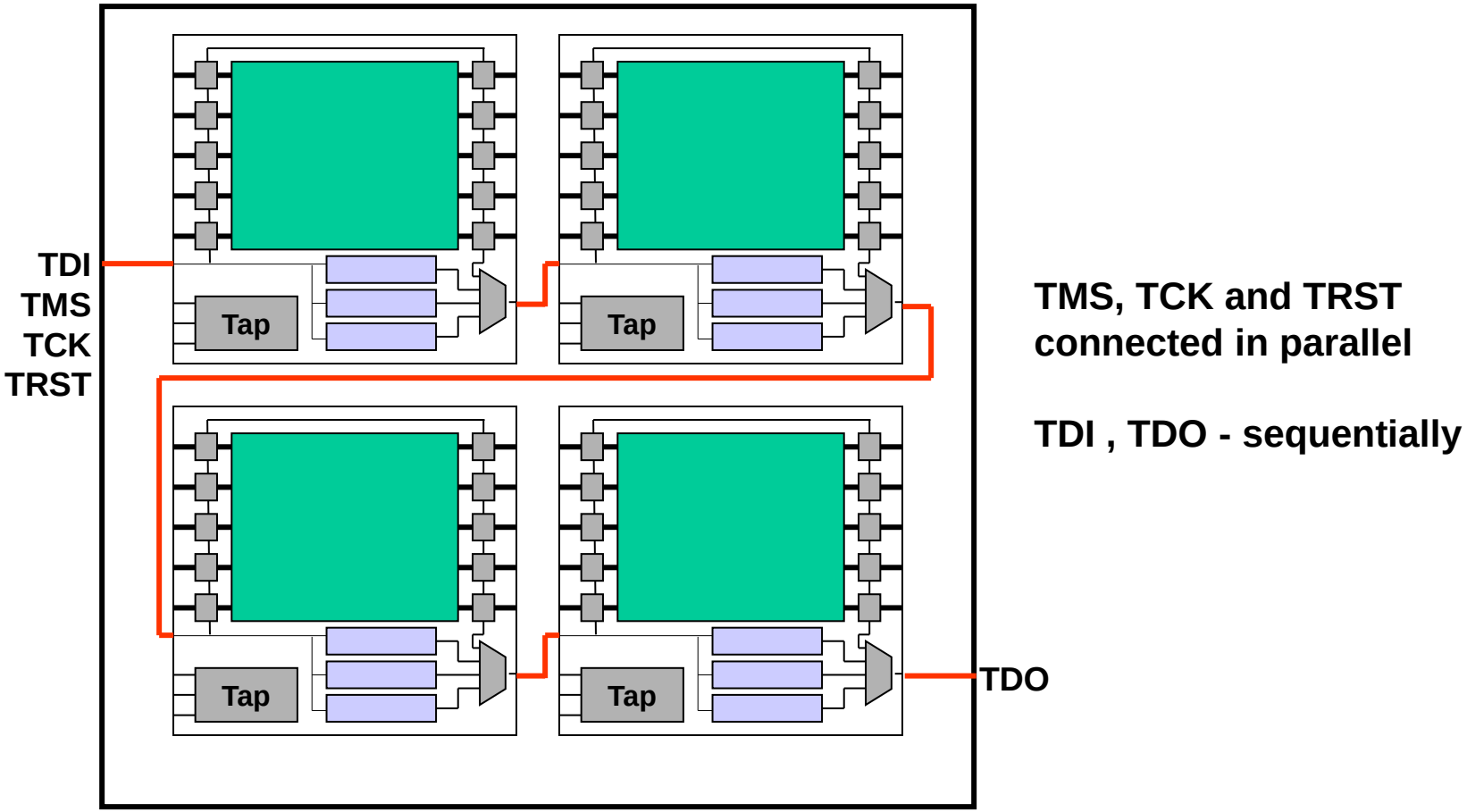
- Intent: Include board-level test functionality into chip-level devices
- Solution: Use serial shift register wrapped around the boundary of chip
- Operation Modes:
  - ✓ Serial Shift mode
  - ✓ Parallel Capture / Update mode



Boundary Scan Architecture



PCB with IEEE 1149.1 test bus

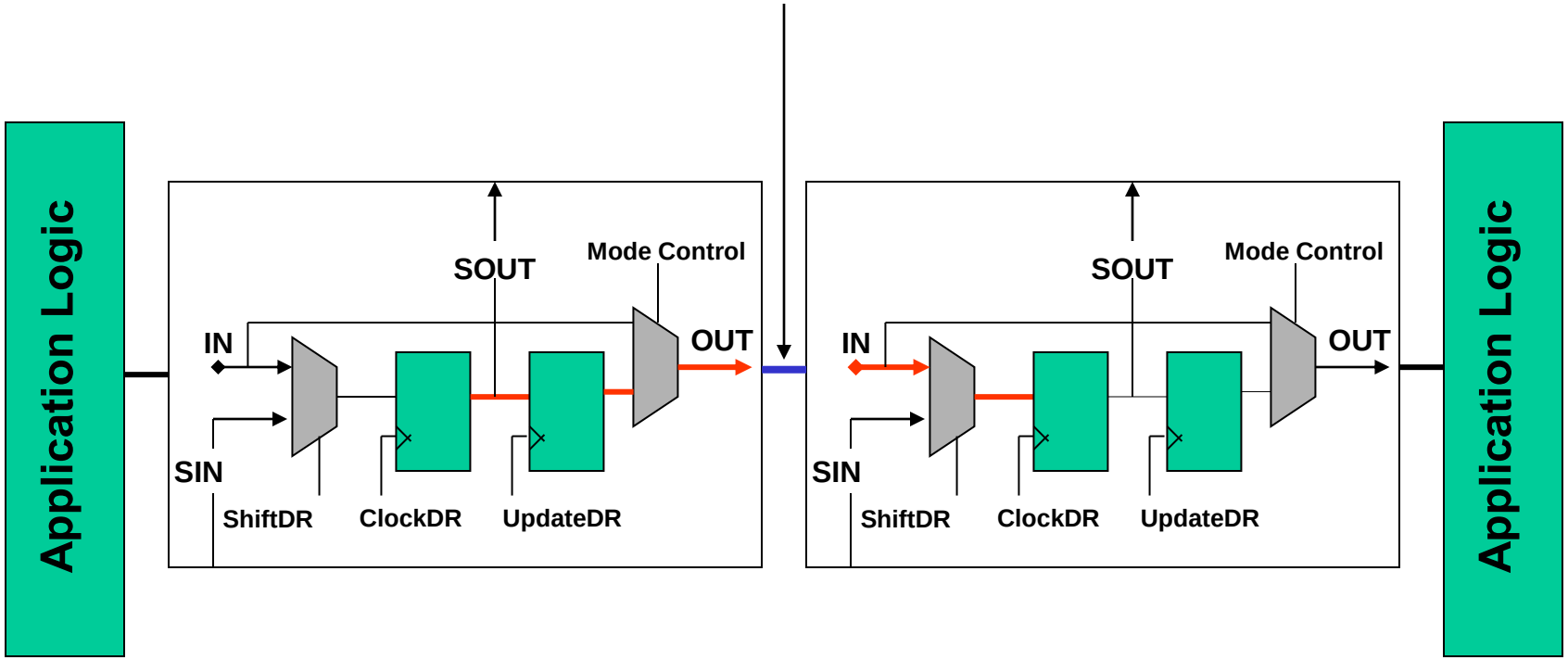


Test Bus Signals

- **TCK** – Test clock, the master clock during the boundary-scan process
- **TDI** – Test Data Input, used to shift in Data or Instructions
- **TDO** – Test Data Output, used to shift out Data
- **TMS** – Test Mode Selector, used to control FSM in TAP Controller
- **TRST** – Optional TAP Controller asynchronous reset

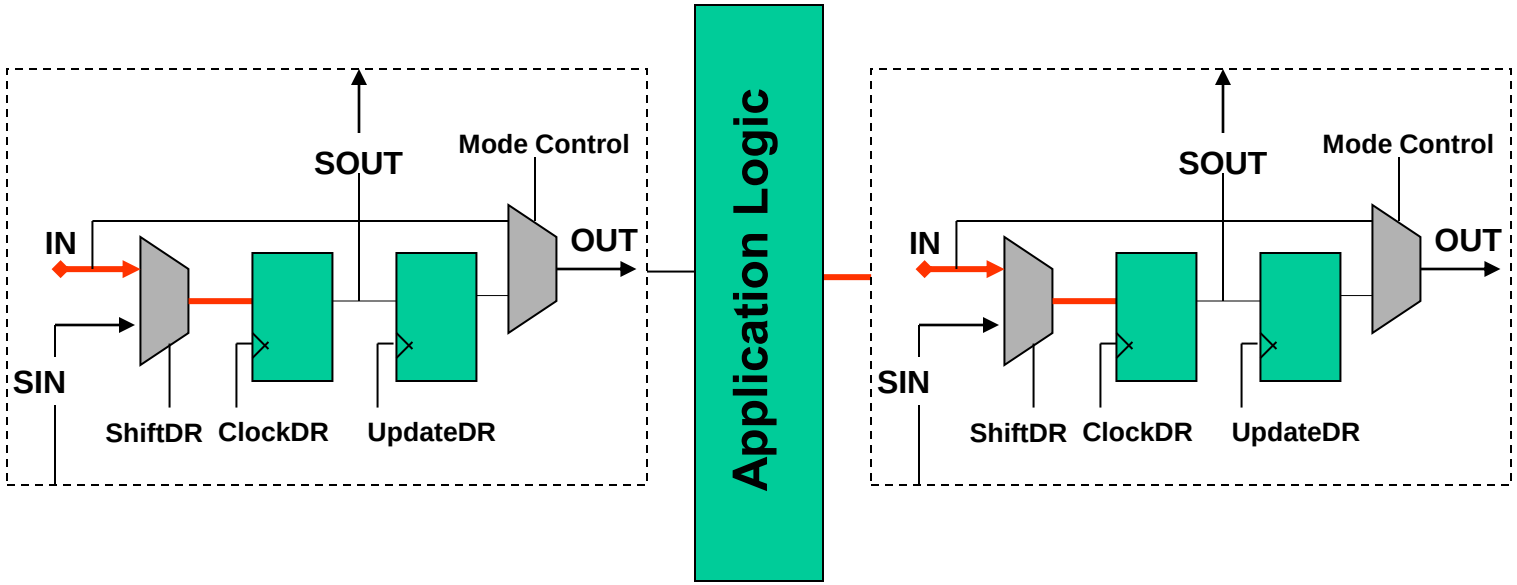
Board and Chip Test Modes

- External Test Mode – to test board interconnect:



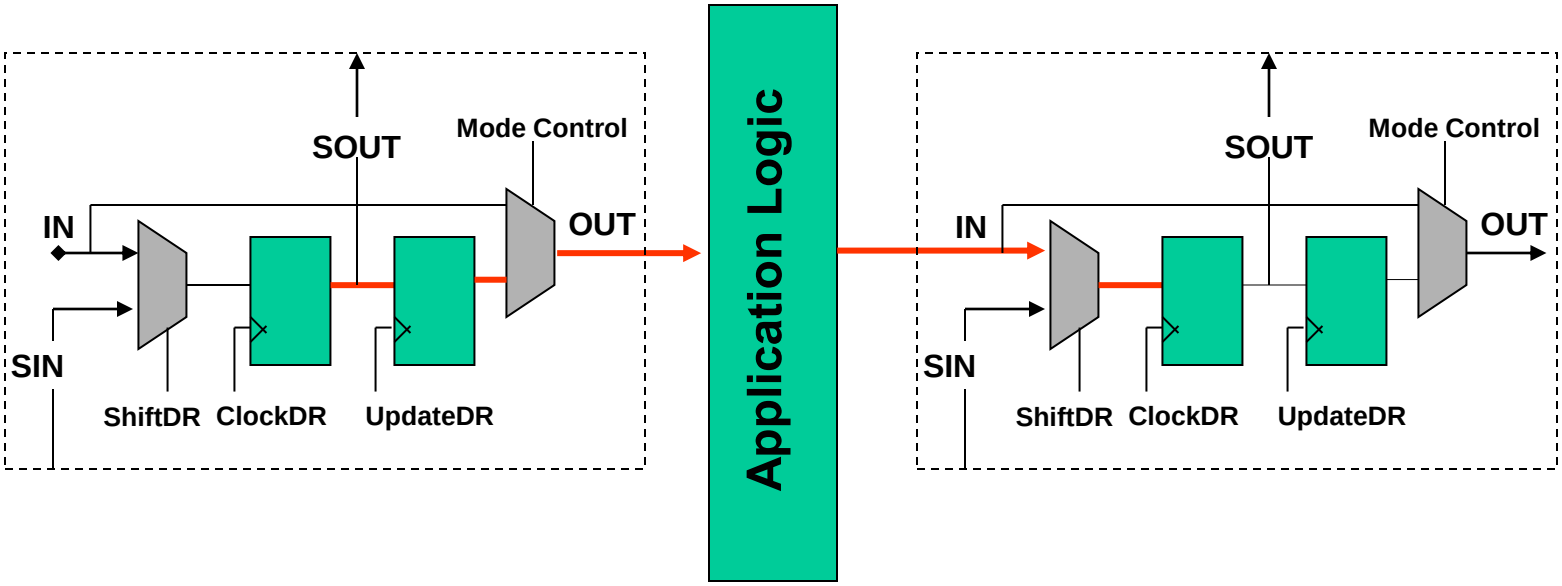
Board and Chip Test Modes (Cont)

- Sample Test Mode: Sampling Data during normal chip operation:



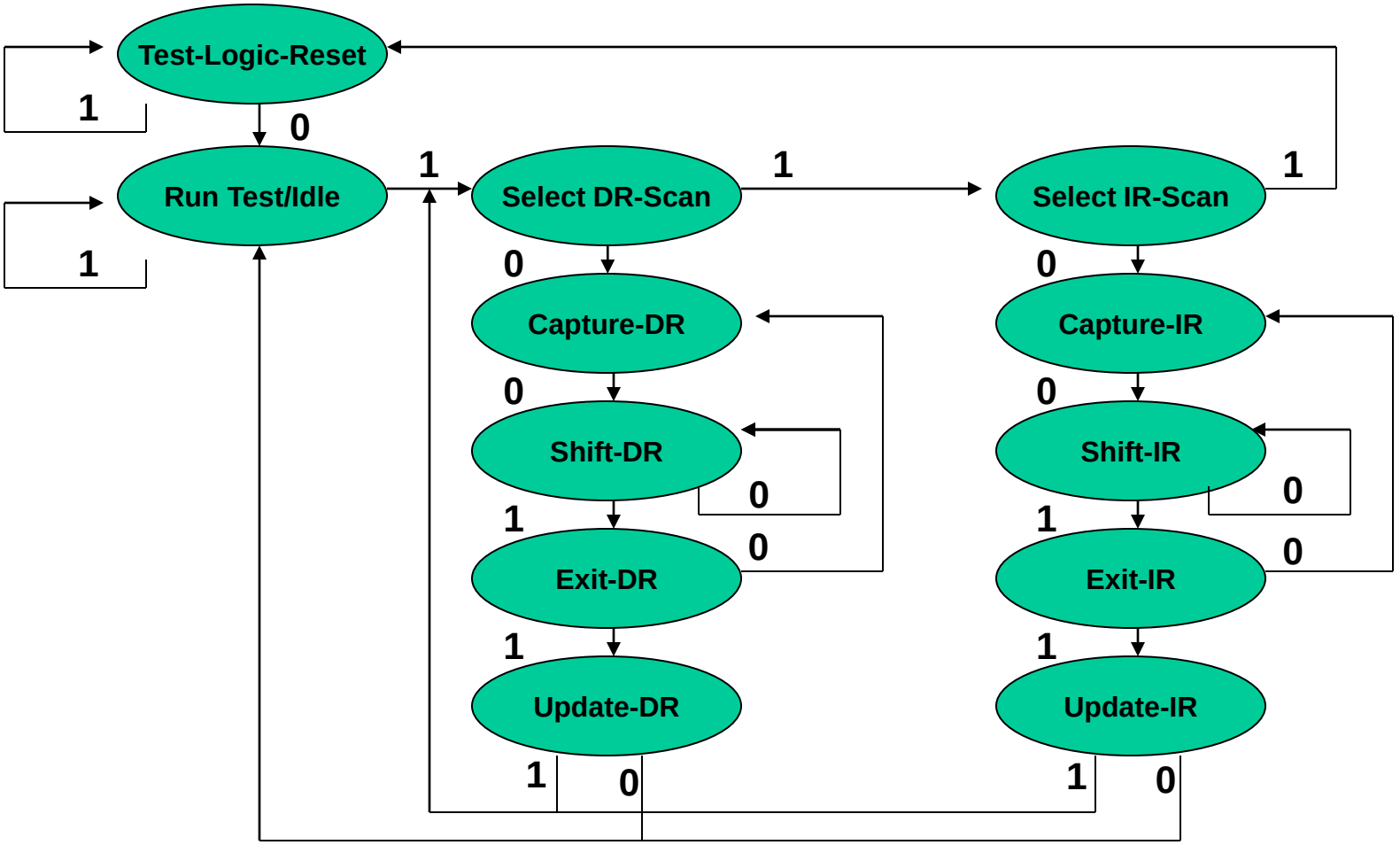
Board and Chip Test Modes (Cont)

- Internal Test Mode: drive chip inputs and capture chip outputs using boundary registers (Functional Isolation)



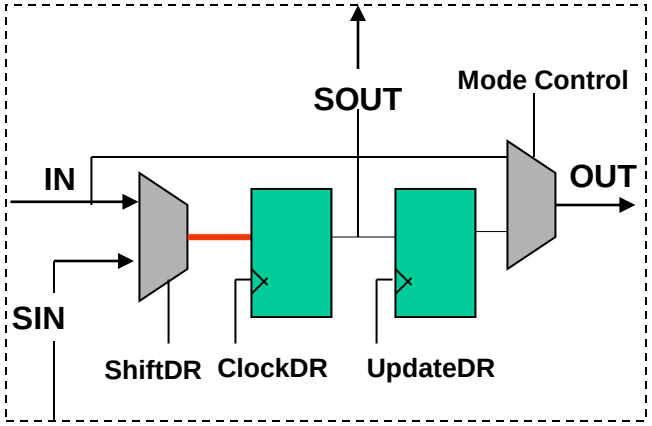
Tap Controller

- FSM of Tap Controller is controlled by only one signal, TMS:



Tap Controller States

- **Test-Logic-Reset :** Boundary Scan disabled, normal functional mode
- **Run Test/Idle :** Internal BIST test runs
- **Capture-DR :** Data loaded in parallel into TDR (Test Data Register) selected by current instruction (ClockDR pulse, ShiftDR = 0)
- **Shift-DR :** Shift Data in TDR, selected by current instruction (ClockDR pulse, ShiftDR = 1)
- **Update-DR :** Update data on the output of TDR, selected by current instruction (UpdateDR pulse)



TAP Controller Instructions

- **Bypass**: to bypass current chip, when targeting the other one
- **Highz**: turns all device output off and inserts the bypass register between TDI and TDO.
- **Clamp**: the contents of the boundary register control the state of output pins while the bypass register is connected between TDI and TDO
- **Extest** : to test circuitry external to the chip (board interconnect)
- **Sample**: sample data on IO Pads into the boundary register
- **Intest**: To apply a test vector to the chip via boundary-scan path and capture logic response
- **RunBIST**: Allows self-test execution on the chip

Built-in Self-Test (BIST)

BIST - Capability of a circuit to test itself

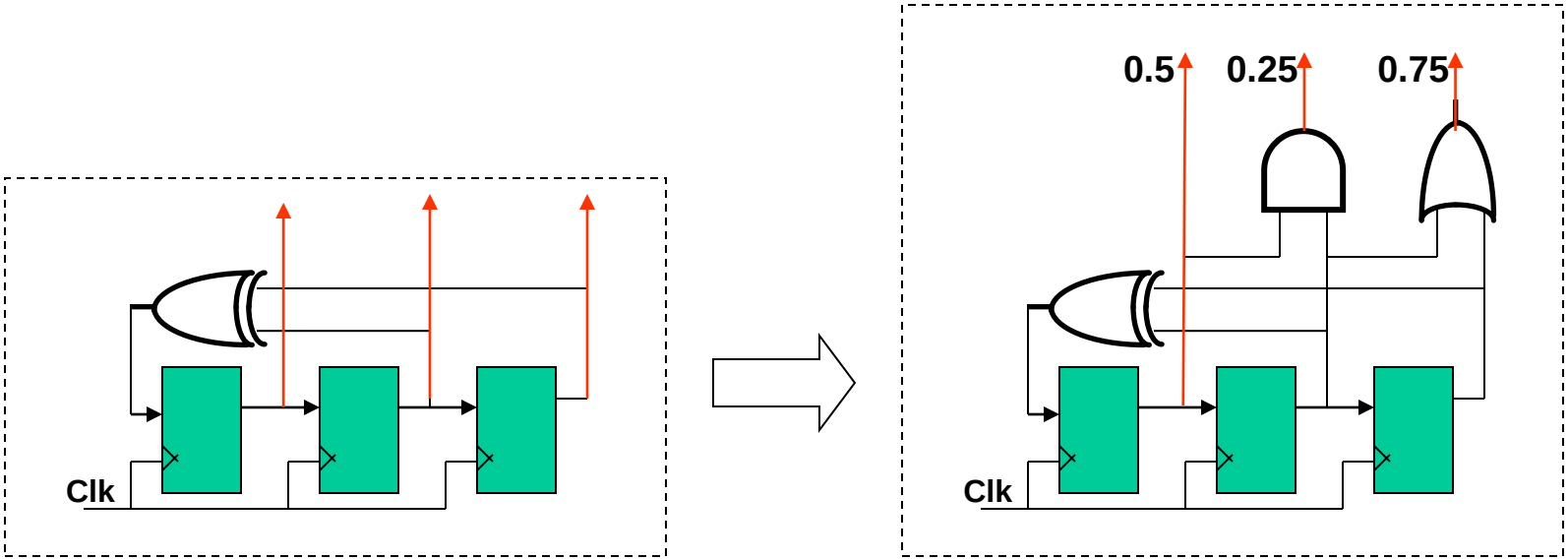
Test Pattern Generation Types:

- ✓ **Exhaustive Testing (for n inputs, 2^n tests)**
- ✓ **Pseudorandom Testing (weighted Test Generation)**
- ✓ **Pseudoexhaustive Testing (divide by logic cones and test them in parallel, but each one exhaustively)**

- **Pseudo Random Pattern Generator (PRPG) – multioutput device that generates pseudorandom output patterns (based on LFSR, Linear Feedback Shift Register)**
- **Multiple-Input Signature Register (MISR) – multi-input device that compresses a series of input patterns into unique signature**

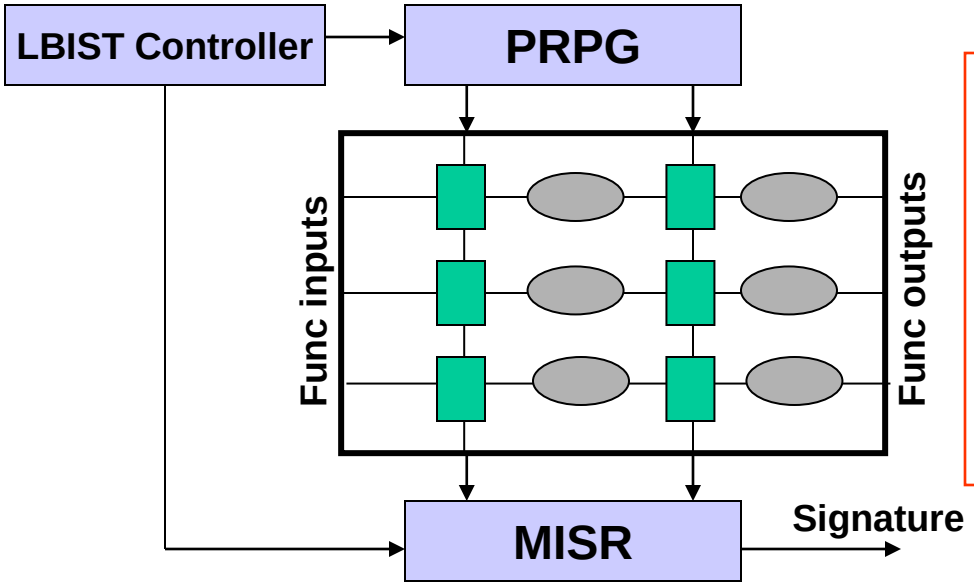
Weighted PRPG

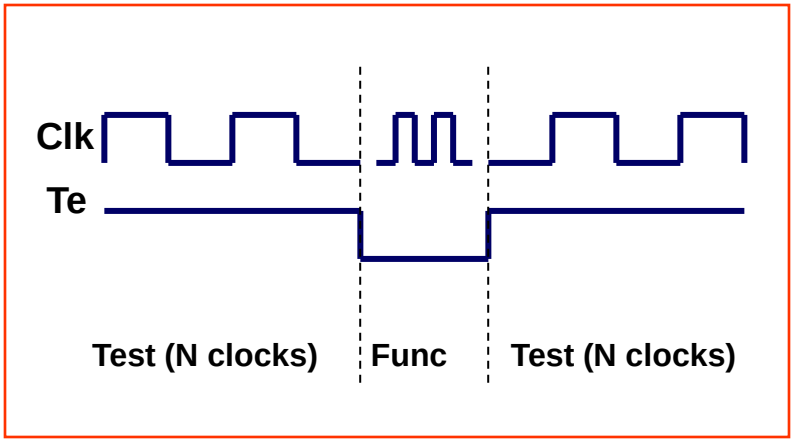
- PRPG: produces pseudorandom data without replacement (all vectors are unique).
- Constant-Weight PRPG: probability to get “1” for each output is constant (Example : equal number of “1” and “0” in each word => weight = 0.5)
- PRPG can adjust weights adding combinatorial logic to the outputs:



Generic LBIST Architecture

- First, PRPG issues N pseudorandom tests, where N – maximal internal scan chain length.
- Second, series of Functional Clock pulses is issued
  - ✓ for DC test, the same test clock as for PRPG is used
  - ✓ For AC test, functional clock must be provided with real frequency
- Third, changed data is shifted to MISR and compressed signature is created (using the same N number of test clocks)





LBIST Design Issues

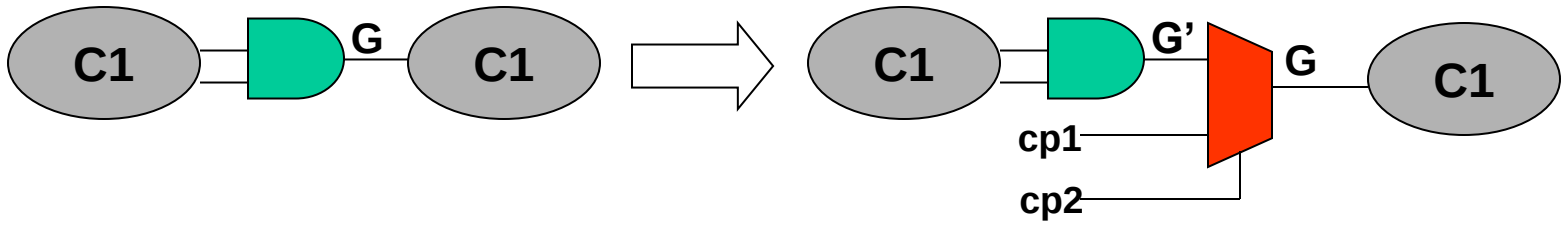
- In order to produce constant signature, we need to remove all X – sources from design:
  - ✓ Assign constant logic value to all Primary Inputs
  - ✓ Isolate memories (or all elements without scan chains)
  - ✓ Isolate PLLs
- LBIST can be initiated and signature can be read out using user-defined instructions of TAP controller
- Long simulation times to produce signature – use of cycle-based simulator

TPI – Test Points Insertion

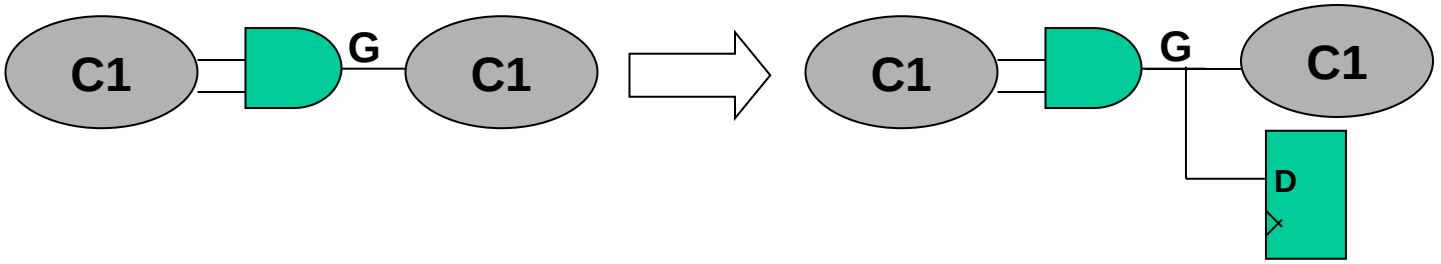
Two type of test points :

- ✓ Control Points (CP) are Primary Inputs or Scannable Register Outputs to enhance controlability
- ✓ Observation Points (OP) are Primary Outputs or Scannable Register Inputs to enhance observability

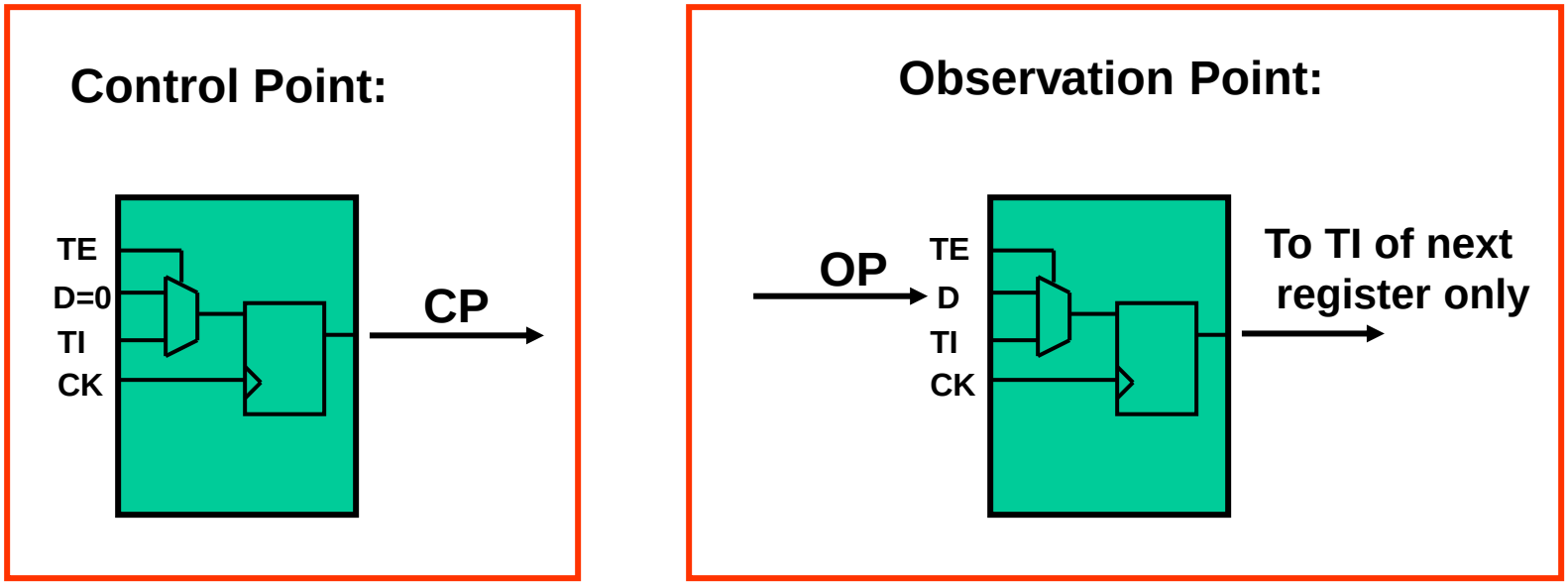
Problem: G not controlable



Problem: G not observable

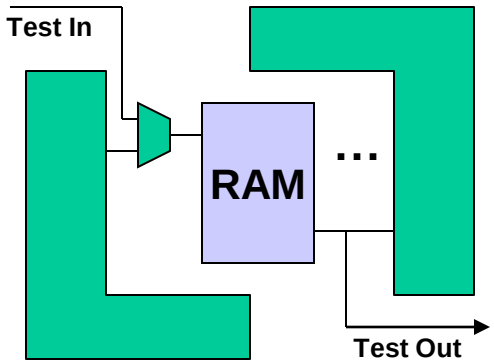


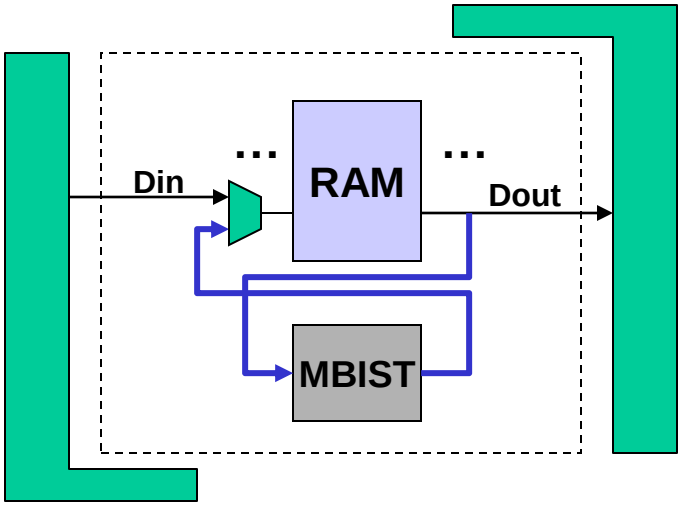
Scannable Register Insertion



Memory BIST

- Embedded Memories use non-scannable registers – how to test them?
  - ✓ Getting access to all memory pins from PI and PO is expensive…
  - ✓ Better solution – add Memory BIST Controller to generate Test Patterns and to observe Test Responses from memory
- Two ways to add controller :
  - ✓ Separate for each memory array (encapsulation) - less wires, more area
  - ✓ Shared for the number of memory arrays - less area, but much more wires
- Memory Test is initiated using TAP Controller

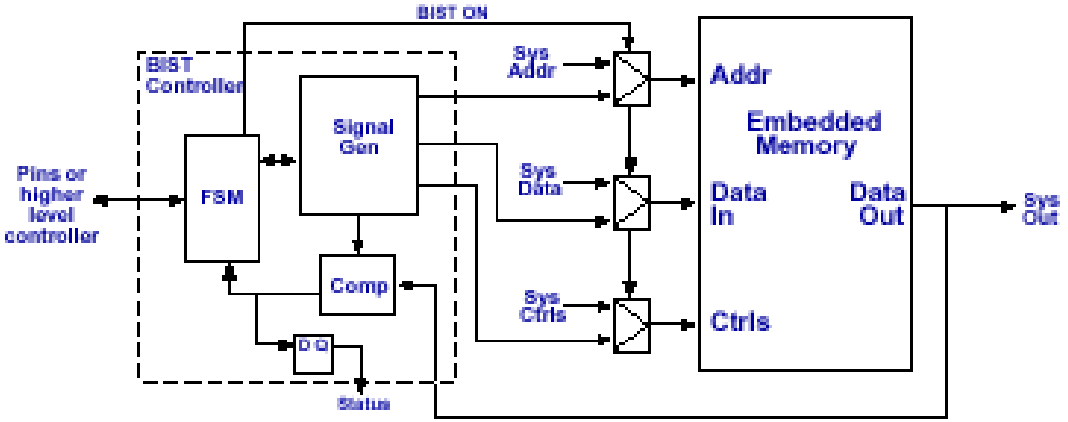




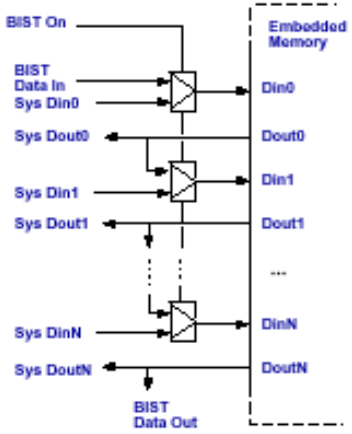
Logic Vision Memory BIST

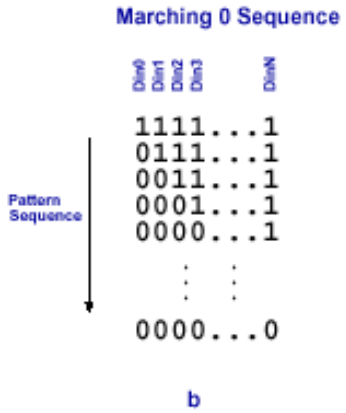
- Logic Vision solution: reducing the number of SRAM test vectors to one:

Parallel Test Vectors:



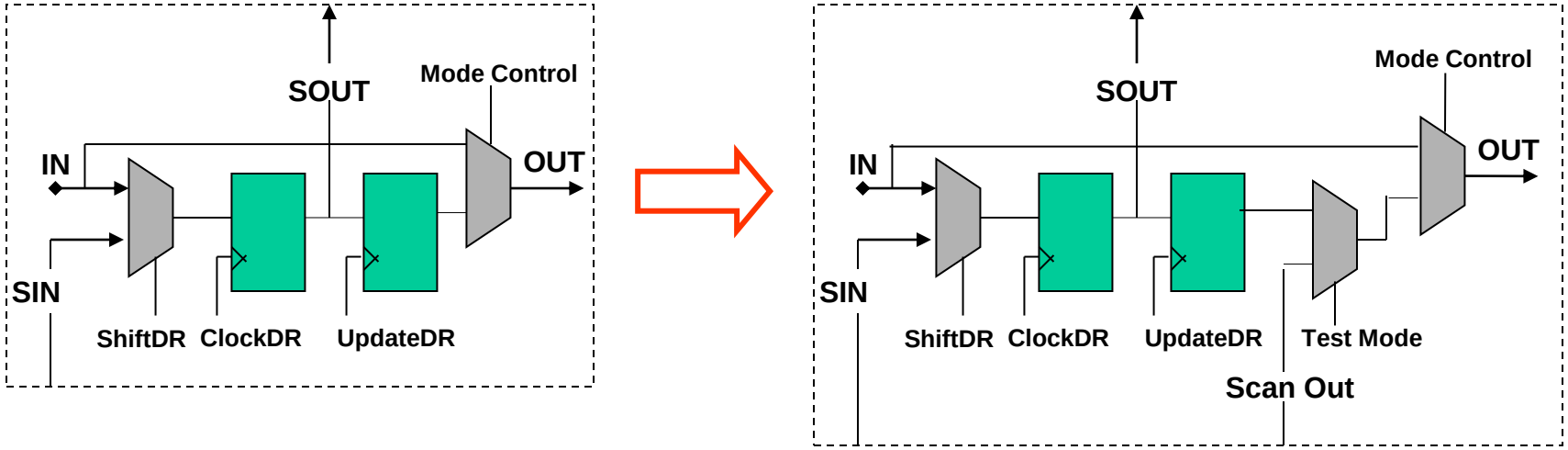
Sequential Test Vectors:





Pin Sharing

- More internal scan chains for faster testing – more test Iopads
- Internal Test Scan Input/Output pads are disconnected on the board
- The pads number in the chip is limited.
- Solution: Share Functional and Test pins



JTAG for functional debugging

Allscan:

- ✓ “Freeze” the chip and get access to ALL registers data
- ✓ Modify Some registers data and and continue in functional mode

Implementation:

- ✓ Serial connection of all Internal Scan chains between TDI and TDO
- ✓ Test Clock is produces from JTAG clock (TCK)
- ✓ Clocks Control – no clock glitches when “freezing” the chip